REMARKS

Applicant has carefully reviewed and considered the Final Office Action mailed on December 16, 2004, and the references cited therewith.

Claims 1, 2, 4, 7, 8, 11-14, 17, 19-21, 23, and 24 are amended, claims 3, 6, 16, 18, 22, and 26-38 are canceled, and no claims are added; as a result, claims 1, 2, 4, 5, 7-15, 17, 19-21, and 23-25 are now pending in this application.

§102 Rejection of the Claims

Claims 1-3, 6, 11-13, 16, 21-23, 26 and 31-33 were rejected under 35 USC § 102(e) as being anticipated by Williams et al. (US 2002/0093356). Claims 3, 6, 16, 22, 26, and 31-33 have been canceled, rendering this rejection moot with respect to those claims.

Claims 1, 11, 21:

Applicants have amended independent claims 1, 11, and 21 to narrow the device under test (DUT) to a microprocessor. Applicants have further amended independent claims 1, 11, and 21 to recite the execution of "software within the FRIT kernel" "by the microprocessor and from the on-board memory of the microprocessor" to make clear that the generation and execution of functional tests is performed by software running on the device under test, and not on the tester or an ATPG tool. Still further, applicants have amended independent claims 1, 11, and 21 to recite executing "software within the FRIT kernel to repeatedly generate and execute functional tests to test the microprocessor". Applicants believe that these amendments and remarks adequately address the issues explained in the "Response to Arguments" section of the Final Office Action in which the rationale is given for maintaining the rejection of independent claims 1, 11, and 21. Accordingly, applicants believe that the rejection of independent claims 1, 11, and 21 under 35 USC § 102(e) as being anticipated by Williams has been overcome. Applicants also believe that the rejection of claims 2, 12, 13, and 23 has been overcome because they depend on the independent claims 1, 11, and 21, which are believed to be in condition for allowance.

§112 Rejection of the Claims

Claim 36 was rejected under 35 USC § 112, second paragraph as indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 36 has been canceled, rendering this rejection moot.

§103 Rejection of the Claims

Claims 4, 5, 7-10, 14, 15, 17-20, 24, 25, 27-30, 34-37 and 38 were rejected under 35 USC § 103(a) as being unpatentable over Williams et al. (US 2002/0093356) in view of Gittinger et al. (U.S. Patent No. 5,668,815). Claims 18, 27-30, 34-37, and 38 have been canceled rendering this rejection moot with respect to those claims.

Claims 4, 5, 7-10, 14, 15, 17, 19, 20, 24 and 25 include, by virtue of dependency, the additional limitations included in independent claims 1, 11, and 21, as amended. Applicants respectfully submit that the combination of Williams and Gittinger does not disclose, teach, or suggest the subject matter of these claims, including for example, "loading the kernel test patterns stored in the tester memory onto an on-board memory of a microprocessor to form the FRIT kernel in the on-board memory of the microprocessor, wherein the FRIT kernel includes a software built-in self-test engine (SBE)," and executing or enabling execution "by the microprocessor and from the on-board memory of the microprocessor of software within the FRIT kernel to repeatedly generate and execute functional tests to test the microprocessor."

At the end of the first full paragraph on page 10 of the office action, the Examiner takes the position that it would have been obvious to move the test sequence generation and execution functions to the DUT, and that the artisan would be motivated to do so because Williams suggests testing circuitry (LFSR 230, pg. 5 para 46) can be incorporated on the DUT. Applicants respectfully disagree. The LFSR of Williams is a shift register in the tester. The cited paragraph of Williams suggests moving a shift register from the tester to the device under test. Applicants take the position that one skilled in the art will not read this suggestion of relocating a shift register and arrive at loading a FRIT kernel onto the device under test to be executed by the device under test to generate and execute test sequences.

Applicants respectfully submit that the rejection under 35 USC § 103(a) has been overcome, and that the claims are in condition for allowance.

Canceled claims

Applicants have canceled a significant number of claims in this response. Cancellation of claims should not be construed as related to patentability, in part because many claims were canceled to reduce filing fees that have increased considerably between the application filing date and the date of this response.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (952-473-8800) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-2359.

Respectfully submitted,

PRAVEEN PARVATHALA

By his Representatives,

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Date 3-14-05 By Dana B LeMoine
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop RCE, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 14 day of March, 2005.

Jane E. Sagers

Name

Signature